SEMICONDUCTOR PACKAGE AND FABRICATING METHOD THEREOF

ABSTRACT OF THE DISCLOSURE

A semiconductor package and its fabricating method are proposed, in which a plurality of passive devices are integrated under a semiconductor chip, so as to increase the layout number of the passive devices in the semiconductor package and enhance the flexibility of substrate routability, as well as reduce an occupied area of a substrate for miniaturize the semiconductor package in profile. Moreover, as the integrated passive devices are further encapsulated by using an insulative material prior to a molding process, the dislocation of the passive devices caused by a high temperature and mold flow of a molding resin can be prevented from occurrence during molding. Furthermore, the encapsulated passive devices are prevented from contacting bonding wires, allowing the occurrence of short circuit to be avoided and quality of the packaged product to be assured.

* * * * *